EE 434 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Final Exam
Fall 2006

Instructions. Students may bring 3 pages of notes to this exam. There are 9 questions and 8 problems. The points allocated for each question are as indicated. The problems are all worth 10 points. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, and $\gamma = 0$. If reference to a bipolar process is made, assume this process has key process parameters $J_S=10^{-15}A/\mu^2$, $\beta=100$ and $V_{AF}=\infty$. If any other process parameters are needed, use the process parameters associated with the process described on the last page of this exam. Specify clearly what process parameters you are using in any solution requiring process parameters.

1. (2 pts) What is the purpose of the buried collector in a bipolar process?

2. (2 pts) Why has the field oxide growth that was common for isolation in larger feature size processes been replaced with trench isolation in processes with finer feature sizes?

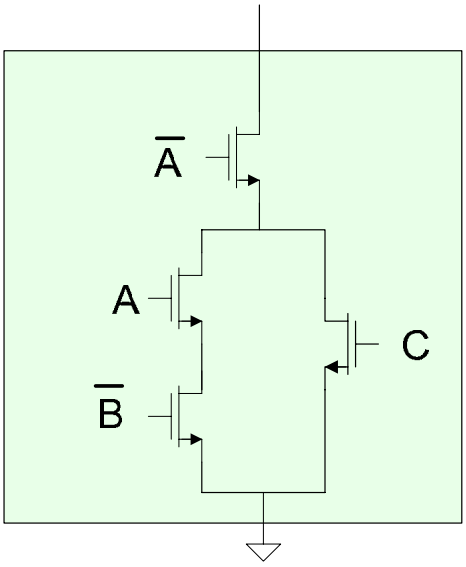
3. (2 pts) Dynamic logic offers potential for a decrease in power dissipation, an increase in speed, and a reduction in area when implementing Boolean functions. There are, however, several challenges. Beyond the need for clocks and the fact the output is valid only during the evaluate state, give two of the major challenges that contribute to the limited use of dynamic logic gates.

4. (2 pts) What is the major difference between an epitaxial silicon layer and a polysilicon layer?

5. (2 pts) Although not formally developed in the lectures, how many small-signal parameters are there in the small-signal model for an arbitrary 5-terminal device?

6. (2 pts) What is the major reason the pull-up resistance for a minimum-sized p-channel transistor is larger than the corresponding pull-down resistance for a minimum-sized n-channel transistor?

7. (4 pts) The pull-down network for a complex logic gate is shown Size the devices so that the worst-case pull-down resistance will be that same as that of a reference inverter driving the same load.



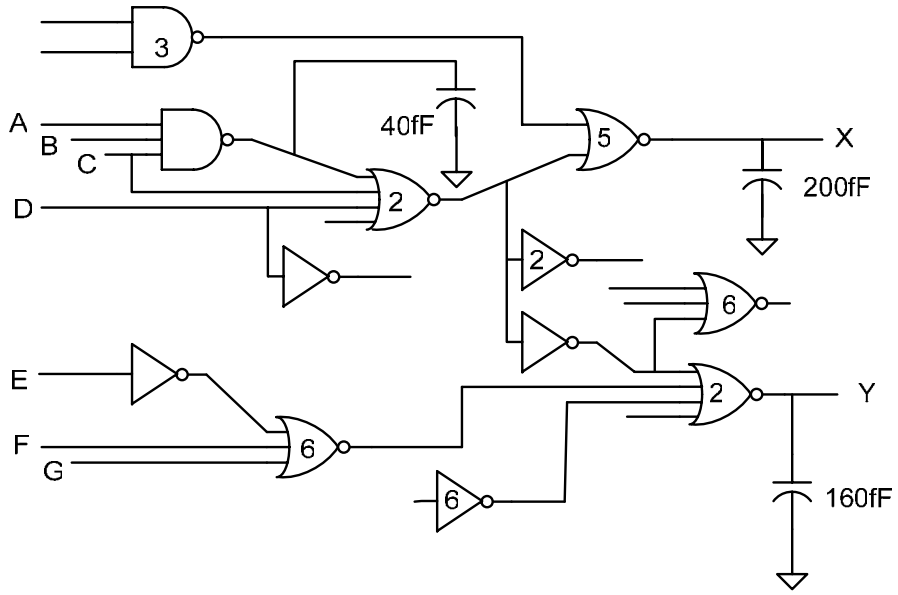
8. (2 pts) In addition to W and L, what other device geometry parameters can be entered to characterize a MOSFET ?

9. (2pts) What region of operation of a BJT is analogous to the triode region of operation of the MOSFET?

Problem 1 A logic circuit designed in conventional static CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times, that the input capacitance of an equal rise/equal fall reference inverter is 2fF, and that it has a propagation delay (T_{HL} + T_{LH}) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

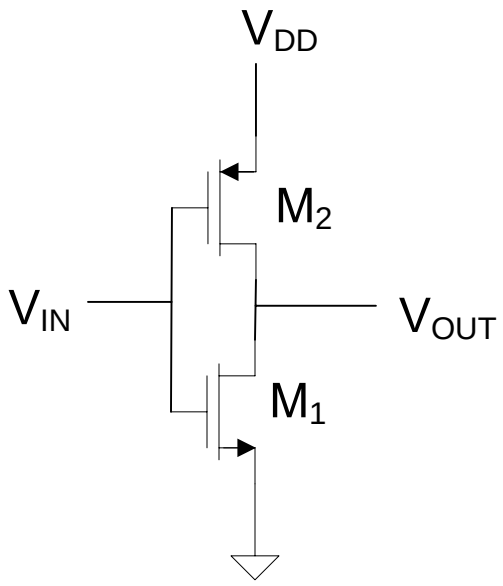
a) Determine the propagation delay (T_{HL} + T_{LH}) from the B input to the X output

b) Repeat part a) if the circuit is comprised entirely of minimum sized devices.



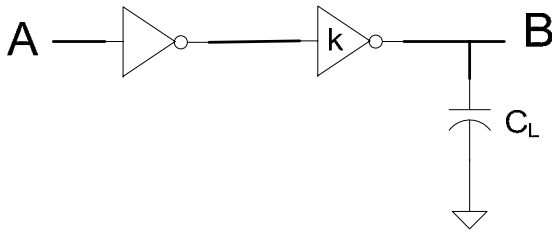
Problem 2 A polysilicon interconnect that is 1mm long and 1um wide is driving 3 uniformly spaced capacitive loads as shown in the figure. Using the Elmore delay model, calculate the propagation delay of a signal from point A to point B in this interconnect bus.

Problem 3 A static CMOS inverter is shown. Assume this is fabricated in a process with V_{TN}=1V, V_{TP}= -2.5V, and that the supply voltage is V_{DD}=4V. Assume further that M_1 and M_2 are minimum-sized with μ_n/μ_p=3.

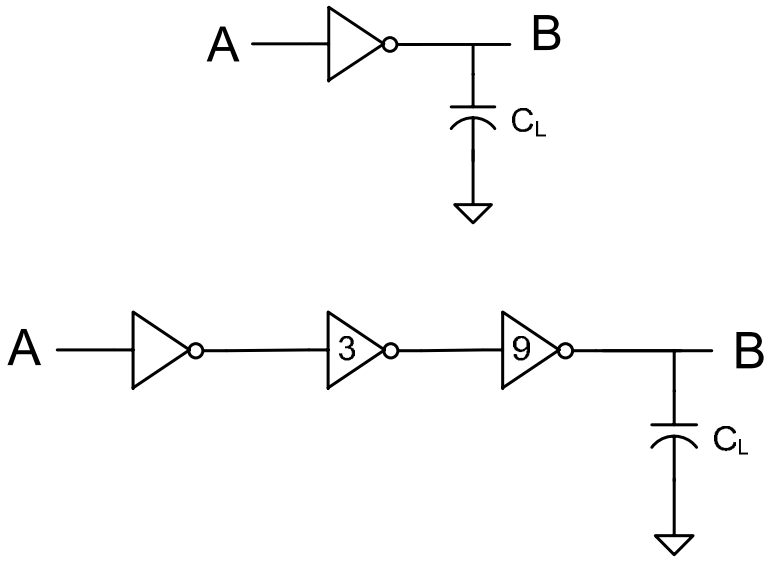


a) Is this a viable digital inverter? Why or why not.
b) If it is a viable digital inverter, determine the trip point
c) If it is a viable digital inverter, size M_1 and M_2 for equal rise and fall times.

Problem 4 Assume a signal propagates from A to B with a capacitive load of C_L=750fF. If the first inverter is sized for minimum-sized equal rise/fall time and the second is an equal rise/fall inverter with an overdrive factor k, determine k so that the propagation delay from A to B is minimized.



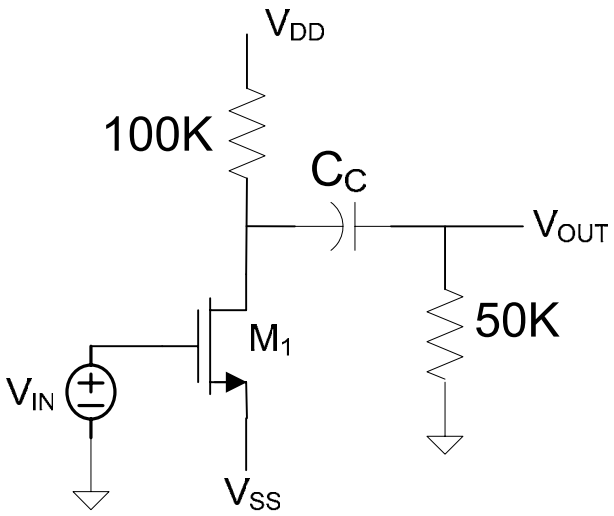
Problem 5 Assume C_{REF} for a minimum-sized equal rise-fall inverter is 2fF and that a total load capacitance of C_L of 54fF is to be driven. In the first scenario, the load is driven directly by a minimum-sized equal rise/fall inverter. Alternatively, it is driven by the much faster two-stage pad driver with OD factors of 3 and 9 respectively. Quantitatively compare the total dynamic power dissipation required to drive C_L by these two different methods. Assume the signal at node A is a clock signal at 200MHz and that V_{DD}=3.5V.



Problem 6 Assume V_{DD}=3.5V , V_{SS}=-1V, and V_{IN} is a small-signal excitation.

a) Size M_1 so that the quiescent drain voltage is 1V

b) With the sizing used in part a), determine the small signal voltage gain if the capacitor C_C is large



Problem 7 Assume the Nonlinear Device is characterized by the model equations

$$I_1 = 2V_1\sqrt{V_2}$$
$$I_2 = 8e^{10V_1} + 2V_2$$

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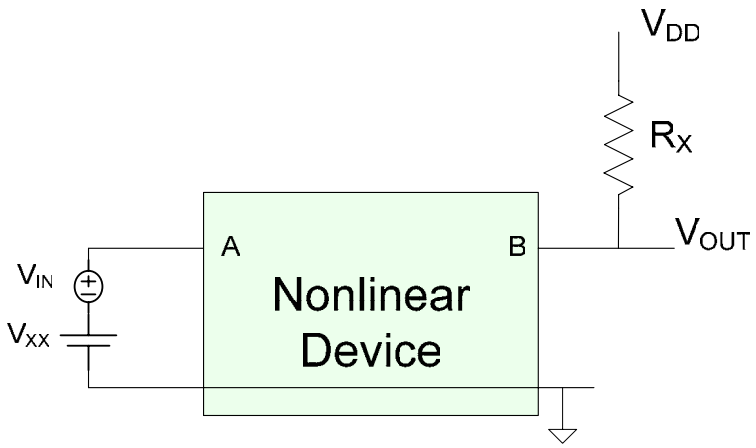
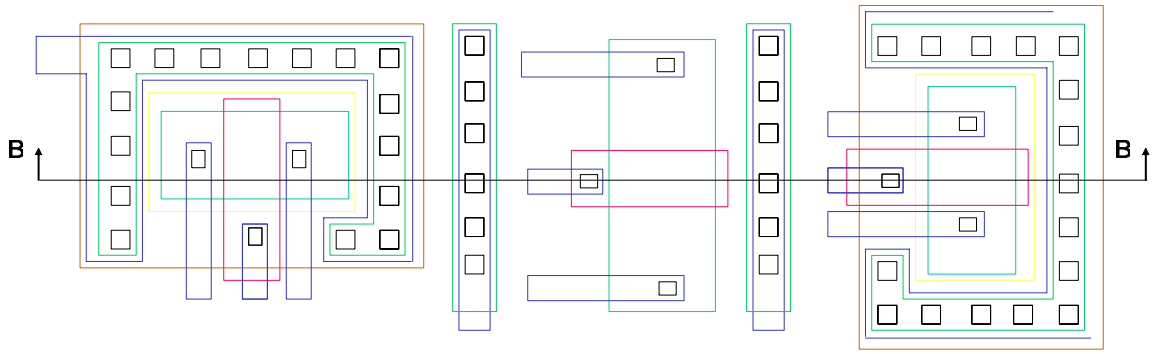
a) Obtain expressions for and draw a small-signal equivalent circuit of this nonlinear device at the Q-point defined by V_{1Q}=0.2V, V_{2Q}=4V.
b) Assume V_{IN} is a small-signal source. Obtain the quiescent output voltage and the small-signal voltage gain of the following circuit if V_{XX}=0.2V, V_{DD}=10V, and R_X= 2 Ω.



Problem 8 The layout of 3 components in a n-well process is shown below. Sketch a cross-section of the wafer along the BB' cross section line indicating all of the relevant features.



Layer Map :

- Active
- n-well
- Poly 1
- Metal
- Contact
- p-select
- Poly 2

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um